REMARKS

Claims 1-21 are pending in the present application.

Reconsideration of the claims is respectfully requested.

35 U.S.C. § 103 (Obviousness)

Claims 1-4, 9-12 and 17-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over "Admitted Prior Art" in view of U.S. Patent No. 3,886,543 to *Marin*. Claims 5-6 and 13-14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over "Admitted Prior Art" in view of *Marin* and further in view of U.S. Patent No. 5,306,963 to *Leak et al*. Claims 7-8 and 15-16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over "Admitted Prior Art" in view of *Marin* and further in view of F.J. Hill et al, *Computer Aided Logical Design With Emphasis On VLSI*. These rejections are respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142, p. 2100-133 (8th ed. rev. 3 August 2005). Absent such a *prima facie* case, the applicant is under no obligation to produce evidence of nonobviousness. *Id.*

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference

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teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *Id.*

The rejection of claims 1-21 under 35 U.S.C. § 103 is improper and should be withdrawn for three reasons. First, the *Marin* reference, directed at debounce logic for a keyboard, is non-analogous art to the claims of the present application, directed to a bus arbitrator (Claim 1), a shared bus system (Claim 9), and a method of activating a plurality of tri-state line drivers in a shared bus system (Claim 17). Second, there is no motivation to combine reference teachings. Third, no reasonable expectation of success in the combination of the references is to be found in the prior art.

The *Marin* reference is directed to debounce logic in a keyboard switch scanner. When a keyswitch is depressed, the contacts bounce. As a result, a switch scanner may sense a series of switch closures before the contacts settle closed. The *Marin* reference teaches that it is advisable for a switch scanner to include means for determining whether a series of sensed switch closures results from contact bounce or from a sequence of successive, deliberate activations of the keyswitch. *See Marin, col. 1, lines 5-37.* In contrast, the claims of the present application are directed to a bus arbitrator for use with circuits that operate on a shared bus driven by buffers having tri-state outputs. The claimed invention eliminates bus contentions by ensuring that the turn-off time of a line driver ceasing to drive the shared bus is shorter than the turn-on time of a line driver beginning to drive the

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shared bus. *See Application, page 6, first paragraph.* As such, the *Marin* reference, directed at sensing mechanical switch contact bounce, is not analogous art to the arbitrator for a shared bus system claimed in the present application.

Furthermore, there is no motivation to combine the cited references as proposed in the Office Action. The *Marin* reference describes the use of two shift register cells and a three-input AND gate, to combine a current sample of keyswitch contact status with two preceding samples. The circuit indicates a switch closure only when three successive samples indicate the switch is closed. The Office Action asserts, however, that a person of ordinary skill would have found it obvious to modify the bus arbitrator of the prior art with a subset of the circuitry of the *Marin* reference—a single shift register cell and a two-input AND gate. The Applicant respectfully submits that the Office Action improperly uses the claims of the present application as a template in selecting portions of the *Marin* reference to combine with the prior art bus arbitrator. Thus, there is no motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine reference teachings as proposed in the Office Action.

Finally, even were a person of ordinary skill to combine portions of the circuitry of the *Marin* reference with the prior art bus arbitrator, as propopsed by the Office Action, no reasonable expectation of success in such a combination may be found in the prior art. While *Marin* describes the benefit of using two shift register cells and a three-input AND gate, it teaches no benefit in using a single shift register cell and a two-input AND gate. As such, the expectation of success in the

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combination of references proposed in the Office Action is found not in the prior art, but in the Applicant's disclosure.

For these reasons, the rejection of claims 1-21 under 35 U.S.C. § 103 is improper and should be withdrawn.

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If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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